REMARKS

Claims 1, 3-6, and 8-16 are pending in the present Application. Claims 1, and 3-5 have been canceled, Claims 6, 11, and 13-16 have been amended, leaving Claims 6 and 8-16 for consideration upon entry of the present Amendment.

Support for the amendment to Claims 6 and 11 can at least be found in Figures 3, 5, and 6 and in the corresponding description in the specification. Additional support can also be found in the specification on page 2, lines 21-27.

With regards to Claims 13 and 15, these claims have each been rewritten in independent form to include all of the limitations of each respective base claim. Further, support for the amendment to Claim 13 can at least be found in Figure 3 and the corresponding description in the specification (e.g., paragraph [0034]).

Claims 14 and 16 have been amended to correct the dependency of the claims.

No new matter has been introduced by these amendments. Reconsideration and allowance of the claims are respectfully requested in view of the above amendments and the following remarks.

Claim Rejections Under 35 U.S.C. § 102(b)

Claims 1 and 5 stand rejected under 35 U.S.C. § 102(b), as allegedly anticipated by U.S. Patent No. 6,133,074 to Ishida et al. ("Ishida").

This rejection is moot, as Claims 1 and 5 have been canceled without prejudice.

Claim Rejections Under 35 U.S.C. § 103(a)

Claims 3-4 stand rejected under 35 U.S.C. § 103(a), as allegedly unpatentable over Ishida.

This rejection is moot, as Claims 3-4 have been canceled without prejudice.

Claims 6, 8-12 stand rejected under 35 U.S.C. § 103(a), as allegedly unpatentable over U.S. Patent No. 6,573,955 to Murade in view of Ishida. Applicants respectfully traverse this rejection.

For an obviousness rejection to be proper, the Examiner must meet the burden of establishing a *prima facie* case of obviousness, i.e., that all elements of the invention are disclosed in the prior art; that the prior art relied upon, coupled with knowledge generally available in the art at the time of the invention, contain some suggestion or incentive that would have motivated the skilled artisan to modify a reference or combined references; and that the proposed modification of the prior art had a reasonable expectation of success, determined from the vantage point of the skilled artisan at the time the invention was made. *In re Fine*, 5 U.S.P.Q.2d 1596, 1598 (Fed. Cir. 1988); *In Re Wilson*, 165 U.S.P.Q. 494, 496 (C.C.P.A. 1970); *Amgen v. Chugai Pharmaceuticals Co.*, 927 U.S.P.Q.2d, 1016, 1023 (Fed. Cir. 1996).

Applicants' independent Claim 6 comprises, *inter alia*, the following elements: "forming a buffer layer over almost the entire surface of the transparent substrate covering the metal layer in an order of a silicon nitride film and a silicon film... the metal layer overlaps regions in which a source, a channel, and a drain of a thin film transistor are to be formed in a first region of the first amorphous semiconductor... wherein the metal layer has a light shielding function for blocking light from a side near the metal layer to the thin film transistor to be formed."

Applicants' independent Claim 11 comprises, *inter alia*, the following elements:

"selectively forming a metal layer above the substrate such that the metal layer is not formed over the formation region of the driver thin film transistor in the driver portion and is present over the formation region of the pixel thin film transistor in the pixel portion, overlapping at least regions in which a source, a channel, and a drain of the pixel thin film transistor are formed... wherein the metal layer has a light shielding function to block light from a side near the metal layer to the pixel thin film transistor to be formed."

In Murade, the polycrystallization of the TFT semiconductor film is achieved not through laser annealing, but through thermal annealing at a high temperature of 600°C to 700°C in a non-oxidizing atmosphere (Col. 11, lines 1-4). Further, Murade fails to disclose that the buffer layer to be formed on the metal layer 7 has a multi-layer structure. As such, Murade does not recognize influences of the thermal leakage in layers below the semiconductor layer to the polycrystallization when the amorphous semiconductor layer is

polycrystallized through laser annealing nor does Murade recognize the alleviation of influences of the metal layer by employing a multi-layer structure for the buffer layer. Accordingly, one of skill in the art would not be motivated to combine the thermal annealing polycrystallization methods of Murade with the laser annealing polycrystallization methods of Ishida. Nevertheless, even if Ishida is combined with Murade, the combined references still fail to teach or suggest each and every element of Applicants' claimed invention.

More particularly, it is noted that Ishida employs laser annealing for polycrystallizing the amorphous semiconductor layer formed on a gate electrode, which has a light shielding characteristic, with a gate insulating film therebetween. However, the gate electrode having the light shielding characteristic is only formed below the channel formation region of the semiconductor layer forming the active layer of the transistor. With such a structure, it is not possible to prevent entrance of light from the side of the metal layer to the source and drain of the thin film transistor in addition to the channel, as claimed by Applicants.

Further, although a gate insulating film having a layered structure of silicon oxide film and silicon nitride film is provided between the gate electrode and the semiconductor layer of Ishida, the grain sizes of polycrystalline silicon differ from each other in a semiconductor region positioned above a tapered section 76b of the gate electrode 76 and in a semiconductor region positioned above a flat section 76a of the gate electrode 76 (Col. 3, lines 33-57). In other words, the problem of the thermal leakage cannot be solved even when a layered structure of a silicon oxide film and silicon nitride film is formed below semiconductor layer, which differs from Applicants claimed invention.

Even if Murade were combined with Ishida, the combined references would still fail to teach or suggest each and every element of Applicants' independent Claims 6 and 11. Accordingly, independent Claims 6 and 11 are not obvious and are allowable over Murade in view of Ishida. Moreover, as dependent claims from an allowable independent claim, Claims 8-10, and 12 are, by definition, also allowable.

Claims 13-14 stand rejected under 35 U.S.C. § 103(a), as allegedly unpatentable over Ishida in view of U.S. Patent No. 5,705,829 to Miyanaga et al. ("Miyanaga"). Claims 15-16

stand rejected under 35 U.S.C. § 103(a), as allegedly unpatentable over Murade in view of Ishida and Miyanaga. Applicants respectfully traverse this rejection.

Murade and Ishida are each silent to teaching or suggesting that the grain sizes of the polycrystalline semiconductors formed in the first region and in the second region through laser annealing are within an appropriate range and different from each other. Rather, in making the rejection, the Examiner relied upon Miyanaga for teaching this element. However, it is noted that Miyanaga explicitly discloses that "only the region of the semiconductor film which corresponds to the peripheral circuit region is irradiated with a laser light 216 in order to improve the crystallinity") in a separate annealing process (Col. 4, line 61 to Col. 5, line 4).

In other words, the above cited references either alone or in combination fail to teach or suggest that polycrystalline semiconductor layers having "appropriate and different grain sizes" are formed both in a region of the first amorphous semiconductor layer below which a metal layer is formed and the region of the second amorphous semiconductor layer below which no metal layer is formed, through a laser annealing process of the same step (i.e., without applying a separate annealing process to the drive portion as described in Miyanaga).

Furthermore, it is noted that Miyanaga discloses a thermal annealing process for crystallizing the amorphous silicon in the region of the thin film transistor of the pixel section and in the region of the thin film transistor of the driver circuit section, instead of a laser annealing process claimed by Applicants. Furthermore, Miyanaga fails to disclose formation of a light shielding layer below the active layer of the thin film transistor.

For at least these reasons, each and every element of independent Claims 13 and 15 are not taught or suggested by the above-cited references. As such, independent Claims 13 and 15 are not obvious and are therefore allowable over Ishida, Murade, and Miyanaga. Moreover, as dependent claims from an allowable independent claim, Claims 14 and 16 are, by definition, also allowable.

It is believed that the foregoing amendments and remarks fully comply with the Office Action and that the claims herein should now be allowable to Applicants. Accordingly, reconsideration and allowance are requested.

If there are any additional charges with respect to this Amendment or otherwise, please charge them to Deposit Account No. 06-1130.

Respectfully submitted,

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